6.8 A Bandpass ΔΣ DDFS-Driven 19GHz Frequency Synthesizer for FMCW Automotive Radar

Hoon Hee Chung[1], Umar Lyles[2], Tino Copani[1], Bertan Bakkaloglu[1], Sayfe Kiaei[1]

[1]Arizona State University, Tempe, AZ
[2]Texas Instruments, Melbourne, FL

The field of automotive radar has been developed for intelligent transport systems (ITS) and autonomous cruise control (ACC) systems by using discrete GaAs components to fulfill the specification of the 76GHz standard. Reducing cost and achieving a smaller board area are making fully integrated automotive radar systems highly desirable. In this paper, a DSP compatible 19GHz frequency synthesizer that is fabricated in a 0.25μm SiGe process is presented. The radar transmitter requires only a single external pHEMT multiply-by-4 frequency multiplier to produce a 76GHz triangular frequency-modulated continuous-wave (FMCW) signal compliant with automotive radar transmitter specifications.

FMCW transmitters require a low phase noise for a wide range of chirping frequencies in order to achieve a fine range resolution. To implement an FMCW synthesizer, a fractional-N phase-locked loop (PLL) or a hybrid PLL using a direct digital frequency synthesizer (DDFS) have previously been proposed [1]. For wide frequency chirping ranges, fractional-N PLLs suffer from integer-N boundary fractional spurs, and quantization noise of the DDFS and reconstruction filters degrade their noise performance.

In this work, a digital bandpass-ΔΣ (BPΔΣ) DDFS-driven millimeter-wave integer-N PLL that can achieve a fine frequency chirping linearity and low phase noise is presented. Figure 6.8.1 shows the block diagram of the proposed direct-synthesis 19GHz FMCW transmitter. The BPΔΣ DDFS, with an SFDR independent of the allocated frequency tone within the modulation bandwidth, provides a fine frequency step resolution (less than 1Hz) with fast transition. Quantization noise from digital blocks and spurs are attenuated by using a ΔΣ modulator to tune an injection-locked oscillator (ILO). The low-frequency (37MHz) FMCW signal generated by BPΔΣ DDFS is upconverted to 19GHz by adopting a 9GHz VCO and a monolithic frequency doubler. Finally, an on-board rat-race balun is used to perform differential to single-ended conversion of the PLL output.

The BPΔΣ DDFS has an input frequency control word length of 28 bits provided by the DSP. The input code determines the FMCW chirping rate, setting the phase increment information to the ROM. The phase information is transformed to amplitude by the quarter-wave look-up table (LUT) providing an FMCW ranging between 18.25 to 18.75MHz. 16b amplitude data out of the LUT is fed into a single-bit tracking BPΔΣ noise-shaper. The block diagram of the BPΔΣ modulator together with the ILO is shown in Fig. 6.8.2. A 2nd-order bandpass noise transfer function (NTF) is adopted in the ΔΣ modulator. Phase increment information is used to set the value of the coefficient α ensuring the zero location of the ΔΣ NTF tracks the DDFS output. In the proposed architecture, 2nd-order locking is exploited to tune a 37MHz free-running frequency oscillator using the ΔΣ DDFS output, thus eliminating the DAC and reconstruction filter.

As shown in Fig. 6.8.2, the bipolar LC-tank ILO receives the 1b ΔΣ output through current injectors Mnj1-2 and Mpj1-2. Bipolar devices are used in the ILO core to reduce the contribution of their flicker noise. The flicker noise of the current-injection transistors is less important as they are switched at the DDFS clock frequency (150MHz). The ILO locks and tracks the noise-shaped chirping frequency in the vicinity of its free-running frequency [2]. The ILO locking range can be changed by setting the ratio between the injection current and the oscillator core current through S1 and S2 switches. Depending on the output chirping frequency deviation, a 250kHz single-side locking-range is required from a 37MHz center frequency.

A digital phase/frequency detector (PFD) detects the low-noise and low-frequency FMCW signal at the input. To reduce reference spurs, zero dead-zone schemes are applied to the PFD with additional delay blocks on the reset node. A tri-state charge pump (CP) provides the phase-error correction charge to a 2nd-order lead-lag passive loop filter (LPF). The LPF is designed for a 10kHz PLL loop bandwidth, allowing up to a 2kHz FM chirping rate.

The FMCW transmitter uses an integrated 9GHz VCO and frequency doubler, as shown in Fig. 6.8.3. A frequency doubler is preferred in order to overcome the low quality factor of integrated varactors at 19GHz. The VCO consists of a cross-coupled differential pair and enhanced-Q LC-tank. The addition of inductors L_C and capacitors C_C increases loaded Q of the LC resonator (L_T, C_V) centered at 9GHz. Adopted topology allows biasing of the varactor diodes without using resistors. This topology avoids AM-to-PM conversion of low-frequency thermal noise. However, inductor L_C can create unwanted low-frequency oscillations due to decoupling and parasitic capacitors. By using series resistors R_C and degeneration capacitance C_D, it is ensured that the VCO oscillates only at the designed frequency. The VCO core is biased through a current mirror approach. Resistor R_B is placed in the diode-connection path to minimize noise contribution while still avoiding impact on the tank loaded Q.

Frequency doubling is obtained by exploiting common-mode amplification in the BJT pair Q5 and Q6. The coupled inductors, L_1 and L_2, and series capacitors, C_1 and C_2, tune the doubler at the required frequency while minimizing unwanted spurs. The approach of using coupled inductors ensures 180° of phase shift between common-collector and common-emitter signals in spite of the unbalances due to parasitic devices and bonding wires.

The PLL feedback path consists of a high-speed prescaler followed by an integer frequency divider. Divide-by-8 of 9GHz is performed by an E²CL bipolar prescaler and the remaining division is achieved with an asynchronous CMOS divider.

The noise response of the injection-locked reference oscillator is presented in Fig. 6.8.4. By locking the oscillator to the 2nd harmonic of the bandpass ΔΣ output, measured phase noise of the locked oscillator is –96dBc/Hz at 1kHz offset and as low as –125dBc/Hz at 100khz offset from a 37.1MHz reference signal. Measured phase noise of the FMCW transmitter is –113.68dBc/Hz at 1MHz offset frequency from the 19GHz carrier, as shown in Fig. 6.8.5. The FMCW transmitter can provide an output power of –5dBm at 19GHz while drawing 63mA from a 2.5V supply. The VCO provides a 12% tuning range with 930MHz/V VCO gain. The VCO core draws 4.701mA and the doubler draws 5.384mA from a 2.5V supply.

Figure 6.8.6 shows the transient chirp signal after FM demodulation. An FM deviation of 512MHz with a maximum of 200Hz FM rate at the center frequency of 19GHz is achieved. This deviation is measured at the center frequency of 4.73GHz using a high-frequency external divide-by-4 prescaler within 10ms span. The achievable ramp slope is up to 820GHz/s at 76GHz, meeting the FMCW automotive radar specifications. Finally, the transmitter spur level is below –59dBc.

Figure 6.8.7 shows the micrograph of the BPΔΣ DDFS-driven 19GHz frequency synthesizer that is implemented in a 0.25μm SiGe process and occupies 1.5×3mm² of die area.

References:

[1] W. Mayer, M. Meilchen, W. Grabherr, P. Nüchter, R. Gühi, "Eight-Channel 77-GHz Front-End Module With High-Performance Synthesized Signal Generator for FM-CW Sensor Applications," *IEEE Trans. on Microwave Theory and Techniques*, vol. 52, pp. 993-1000, Mar., 2004.
[2] B. Razavi, "A Study of Injection Locking and Pulling in Oscillators," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1415-1424, Sept., 2004.

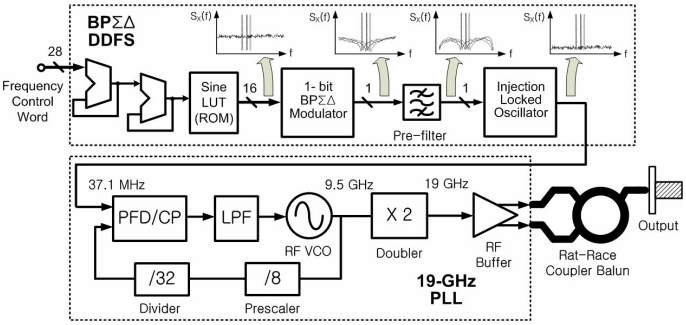

Figure 6.8.1: FMCW transmitter architecture.

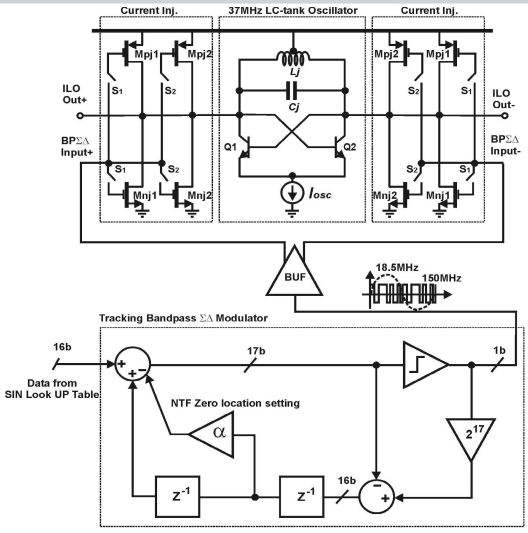

Figure 6.8.2: Tracking band-pass ΔΣ modulator and injection locked oscillator schematic.

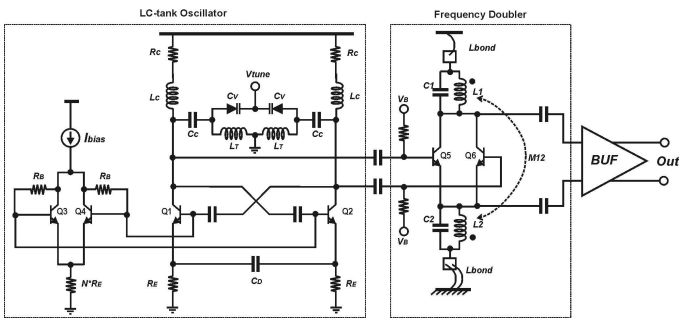

Figure 6.8.3: VCO and frequency doubler schematic.

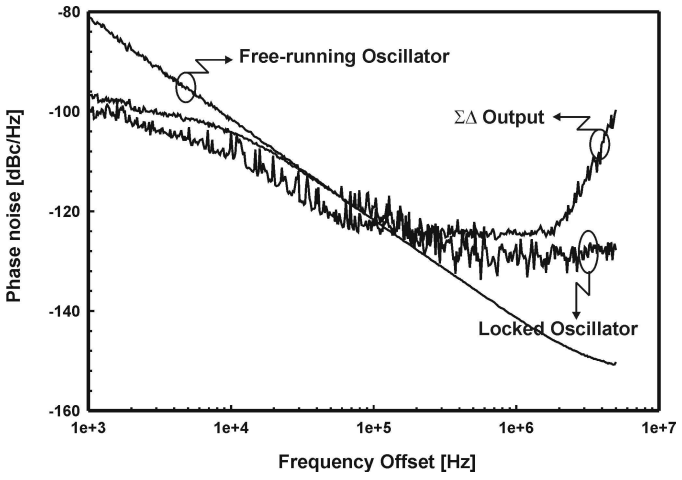

Figure 6.8.4: Band-pass ΔΣ modulator and injection locked oscillator noise response.

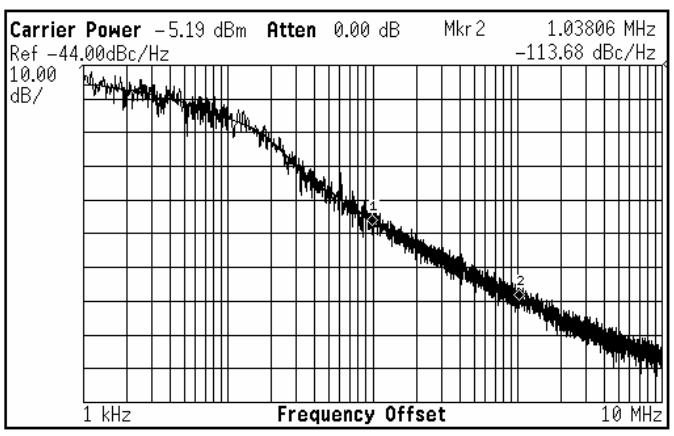

Figure 6.8.5: Phase noise performance of the 19GHz carrier frequency.

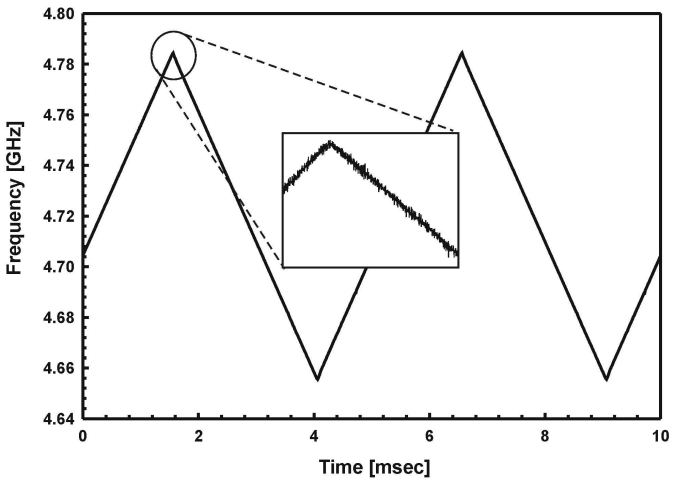

Figure 6.8.6: Transient FMCW frequency response of 512MHz frequency modulation using divide-by-4 external prescaler.

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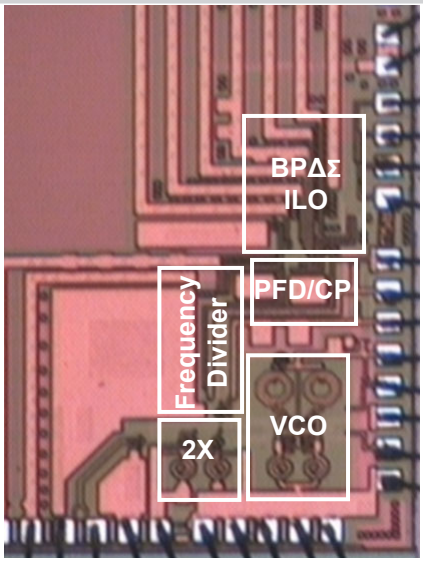

Figure 6.8.7: FMCW transmitter die micrograph.

